

DS3896/DS3897 BTL Trapezoidal™ Transceivers

Check for Samples: [DS3896](#), [DS3897](#)

FEATURES

- 8 bit DS3896 Transceiver Provides High Package Density
- 4 bit DS3897 Transceiver Provides Separate Driver Input and Receiver Output Pins
- BTL Compatible
- Less than 5 pF Output Capacitance for Minimal Bus Loading
- 1 Volt Bus Signal Swing Reduces Power Consumption
- Trapezoidal Driver Waveforms (t_r , $t_f \approx 6$ ns typical) Reduce Noise Coupling to Adjacent Lines
- Temperature Insensitive Receiver Thresholds Track the Bus Logic High Level to Maximize Noise Immunity in both High and Low States
- Guaranteed A.C. Specifications on Noise Immunity and Propagation Delay Over the Specified Temperature and Supply Voltage Range
- Open Collector Driver Output Allows Wire-or Connection
- Advanced Low Power Schottky Technology
- Glitch Free power Up/Down Protection on Driver and Receiver Outputs
- TTL Compatible Driver and Control Inputs and Receiver Outputs

DESCRIPTION

These advanced transceivers are specifically designed to overcome problems associated with driving a densely populated backplane, and thus provide significant improvement in both speed and data integrity. Their low output capacitance, low output signal swing and noise immunity features make them ideal for driving low impedance buses with minimum power consumption.

The DS3896 is an octal high speed schottky bus transceiver with common control signals, whereas the DS3897 is a quad device with independent driver input and receiver output pins. The DS3897 has a separate driver disable for each driver and is, therefore, suitable for arbitration lines. The separate driver disable pins (E_n) feature internal pull ups and may be left open if not required. On the other hand, the DS3896 provides high package density for data/address lines.

The open collector drivers generate precise trapezoidal waveforms, which are relatively independent of capacitive loading conditions on the outputs. This significantly reduces noise coupling to adjacent lines. In addition, the receivers use a low pass filter in conjunction with a high speed comparator, to further enhance the noise immunity and provide equal rejection to both negative and positive going noise pulses on the bus.

To minimize bus loading, these devices also feature a schottky diode in series with the open collector output that isolates the driver output capacitance in the disabled state. The output low voltage is typically "1V" and the output high level is intended to be 2V. This is achieved by terminating the bus with a pull up resistor to 2V at both ends. The device can drive an equivalent DC load of 18.5Ω (or greater) in the above configuration.

These signaling requirements, including a 1 volt signal swing, low output capacitance and precise receiver thresholds are referred to as Bus Transceiver Logic (BTL).



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Logic Diagrams

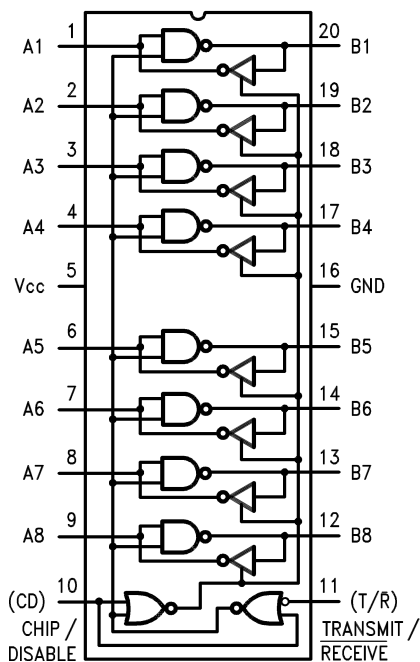


Figure 1. DS3896N, M
See Package Number DW0020B or NFH0020A

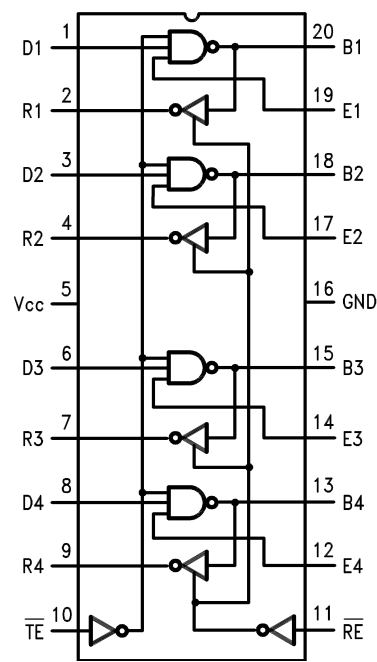


Figure 2. DS3897N, M
See Package Number DW0020B or NFH0020A



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings⁽¹⁾⁽²⁾

Supply Voltage	6V
Control Input Voltage	5.5V
Driver Input and Receiver Output	5.5V
Receiver Input and Driver Output	2.5V
Power Dissipation at 70°C N Package	1480 mW
M Package	TBD mW
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 4 sec.)	260°C

- (1) "Absolute maximum ratings" are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristic" provide conditions for actual device operation.
- (2) If Military/Aerospace specified devices are required, please contact the TI Sales Office/Distributors for availability and specifications.

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage, V_{CC}	4.75	5.25	V
Bus Termination Voltage	1.90	2.10	V
Operating Free Air Temperature	0	70	°C

Electrical Characteristics:⁽¹⁾⁽²⁾

(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver and Control Inputs: (An, Dn, En, CD, T/R, RE, TE)						
V _{IH}	Logical "1" Input Voltage		2.0			V
V _{IL}	Logical "0" Input Voltage				0.8	V
I _I	Logical "1" Input Current	An = Dn = En = V _{CC}			1	mA
I _{IH}	Logical "1" Input Current	An = Dn = En = 2.4V			40	μA
I _{IHC}	Logical "1" Input Current	CD = T/R = RE = TE = 2.4V			80	μA
I _{IL}	Logical "0" Input Current	An = Dn = En = 0.4V		-1	-1.6	mA
I _{ILC}	Logical "0" Input Current	CD = T/R = RE = TE = 0.4V		-180	-400	μA
V _{CL}	Input Diode Clamp Voltage	I _{clamp} = -12 mA		-0.9	-1.5	V
Driver Output/Receiver Input: (Bn)						
V _{OLB}	Low Level Bus Voltage	An = Dn = En = T/R = 2V, V _L = 2V RL = 18.5Ω, CD = RE = 0.8V (Figure 3)	0.75	1.0	1.2	V
I _{IHB}	Maximum Bus Current (Power On)	An = Dn = En = 0.8V, V _{CC} = 5.25V Bn = 2V		10	100	μA
I _{ILB}	Maximum Bus Current (Power Off)	An = Dn = En = 0.8V, V _{CC} = 0V Bn = 2V			100	μA
V _{TH}	Receiver Input Threshold	V _{CC} = 5V	1.47	1.55	1.62	V
Receiver Output: (An, Rn)						
V _{OH}	Logical "1" Output Voltage	Bn = 1.2V, I _{OH} = -400 μA CD = T/R = RE = 0.8V	2.4	3.2		V
V _{OL}	Logical "0" Output Voltage	Bn = 2V, I _{OL} = 16 mA CD = T/R = RE = 0.8V		0.35	0.5	V
I _{OS}	Output Short Circuit Current	Bn = 1.2V CD = T/R = RE = 0.8V	-20	-70	-100	mA
I _{CC}	Supply Current (DS3896)	V _{CC} = 5.25V		90	135	mA
I _{CC}	Supply Current (DS3897)	V _{CC} = 5.25V		50	80	mA

(1) All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.

(2) All typicals are given for V_{CC} = 5V and T_A = 25°C.

DS3896 Switching Characteristics⁽¹⁾

(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver:						
t _{DLH}	An to Bn	CD = 0.8V, T/R = 2.0V, V _L = 2V	5	9	15	ns
t _{DHL}		(Figure 4)	5	9	15	ns
t _{DLHC}	CD to Bn	An = T/R = 2.0V, V _L = 2V	5	10	18	ns
t _{DHLC}		(Figure 4)	5	12	20	ns
t _{DLHT}	T/R to Bn	V _{CI} = An, V _C = 5V, (Figure 7)	5	15	25	ns
t _{DHLT}		CD = 0.8V, RC = 390Ω, CL = 30 pF RL1 = 18Ω, RL2 = NC, V _L = 2V	5	22	35	ns
t _R	Driver Output Rise Time	CD = 0.8V, T/R = 2V, V _L = 2V	3	6	10	ns
t _F	Driver Output Fall Time	(Figure 4)	3	6	10	ns
Receiver:						
t _{RLH}	Bn to An	CD = 0.8V, T/R = 0.8V	5	12	18	ns
t _{RHL}		(Figure 5)	5	10	18	ns

(1) **Note:** NC means open

DS3896 Switching Characteristics⁽¹⁾ (continued)(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver:						
t _{RLZC}	CD to An	Bn = 2.0V, T/ $\overline{R}$ = 0.8V, CL = 5 pF	5	10	18	ns
		RL1 = 390Ω, RL2 = NC, VL = 5V (Figure 6)				
t _{RZLC}		Bn = 2.0V, T/ $\overline{R}$ = 0.8V, CL = 30 pF	5	8	15	ns
		RL1 = 390Ω, RL2 = 1.6k, VL = 5V (Figure 6)				
t _{RHZC}		Bn = 0.8V, T/ $\overline{R}$ = 0.8V, VL = 0V,	2	4	8	ns
		RL1 = 390Ω, RL2 = NC, CL = 5 pF (Figure 6)				
t _{RZHC}		Bn = 0.8V, T/ $\overline{R}$ = 0.8V, VL = 0V,	3	7	12	ns
		RL1 = NC, RL2 = 1.6k, CL = 30 pF (Figure 6)				
t _{RLZT}	T/ $\overline{R}$ to An	VCI = Bn, VC = 2V, RC = 18Ω,	5	10	18	ns
		CD = 0.8V, VL = 5V, RL1 = 390Ω,				
		RL2 = NC, CL = 5 pF (Figure 7)				
t _{RZLT}		VCI = Bn, VC = 2V, RC = 18Ω,	14	24	40	ns
		CD = 0.8V, VL = 5V, RL1 = 390Ω,				
		RL2 = 1.6k, CL = 30 pF (Figure 7)				
t _{RHZT}		VCI = Bn, VC = 0V, RC = 18Ω,	2	4	8	ns
		CD = 0.8V, VL = 0V, RL1 = 390Ω,				
		RL2 = NC, CL = 5 pF (Figure 7)				
t _{RZHT}		VCI = Bn, VC = 0V, RC = 18Ω,	2	8	15	ns
		CD = 0.8V, VL = 0V, RL1 = NC				
		RL2 = 1.6k, CL = 30 pF (Figure 7)				
t _{NR}	Receiver Noise	(Figure 8)	3	6		ns
	Rejection Pulse Width					

DS3897 Switching Characteristics⁽¹⁾(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Driver:						
t _{DLH}	Dn, En to Bn	$\overline{TE}$ = 0.8V, $\overline{RE}$ = 2.0V, VL = 2V	5	9	15	ns
t _{DHL}		(Figure 4)	5	9	15	ns
t _{DLHT}	$\overline{TE}$ to Bn	An = $\overline{RE}$ = 2.0V, VL = 2V, (Figure 4)	5	10	18	ns
t _{DHLT}		RC = 390Ω, VCI = An, VC = 5V, CL = 30 pF	5	12	20	ns
		RL1 = 18Ω, RL2 = NC, VL = 2V (Figure 7)				
t _R	Driver Output Rise Time	CD = 0.8V, T/ $\overline{R}$ = 2V, VL = 2V	3	6	10	ns
t _F	Driver Output Fall Time	(Figure 4)	3	6	10	ns
Receiver:						
t _{RLH}	Bn to Rn	$\overline{TE}$ = 2.0V, $\overline{RE}$ = 0.8V (Figure 5)	5	10	18	ns
t _{RHL}			5	12	18	ns
t _{RLZR}	$\overline{RE}$ to Rn	Bn = $\overline{TE}$ = 2V, VL = 5V, CL = 5 pF	5	10	18	ns
		RL1 = 390Ω, RL2 = NC (Figure 6)				
t _{RZLR}		Bn = $\overline{TE}$ = 2V, VL = 5V, CL = 30 pF	5	8	15	ns
		RL1 = 390Ω, RL2 = 1.6k (Figure 6)				
t _{RHZR}		Bn = 0.8V, $\overline{TE}$ = 2V, VL = 0V,	2	4	8	ns
		RL1 = 390Ω, RL2 = NC, CL = 5 pF (Figure 6)				

(1) **Note:** NC means open

DS3897 Switching Characteristics⁽¹⁾ (continued)

(0°C ≤ T_A ≤ 70°C, 4.75V ≤ V_{CC} ≤ 5.25V unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t _{RZHR}		Bn = 0.8V, $\overline{TE}$ = 2V, VL = 0V,	3	7	12	ns
		RL1 = NC, RL2 = 1.6k, CL = 30 pF (Figure 6)				
t _{NR}	Receiver Noise	(Figure 8)	3	6		ns
	Rejection Pulse Width					
Driver plus Receiver:						
t _{DRLH}	Dn to Rn	$\overline{TE} = \overline{RE} = 0.8V$ (Figure 9)	10	20	30	ns
t _{DRHL}			10	20	30	ns

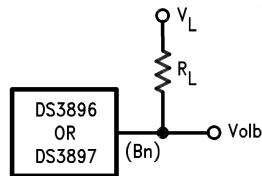
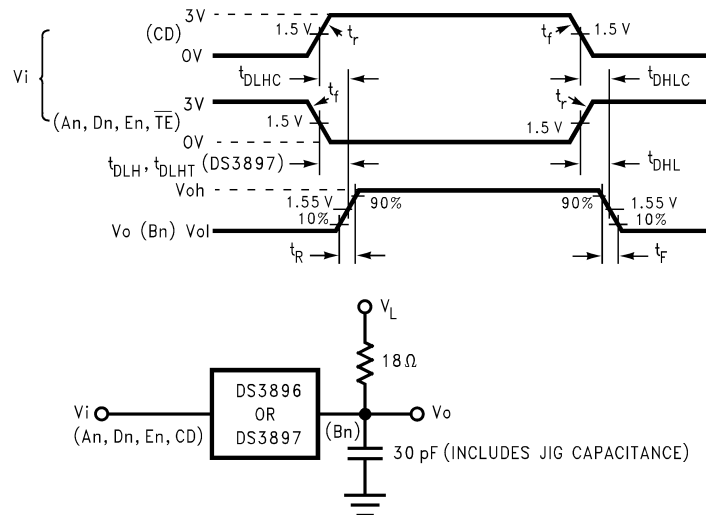
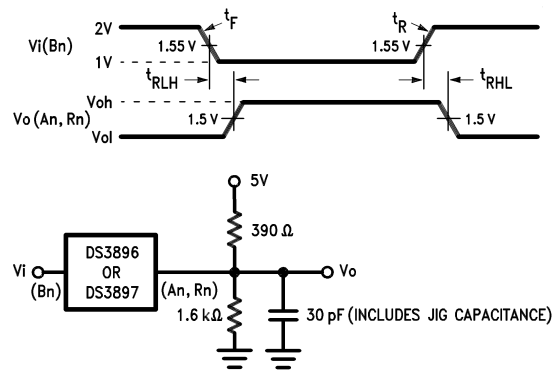


Figure 3. Driver Output Low Voltage Test



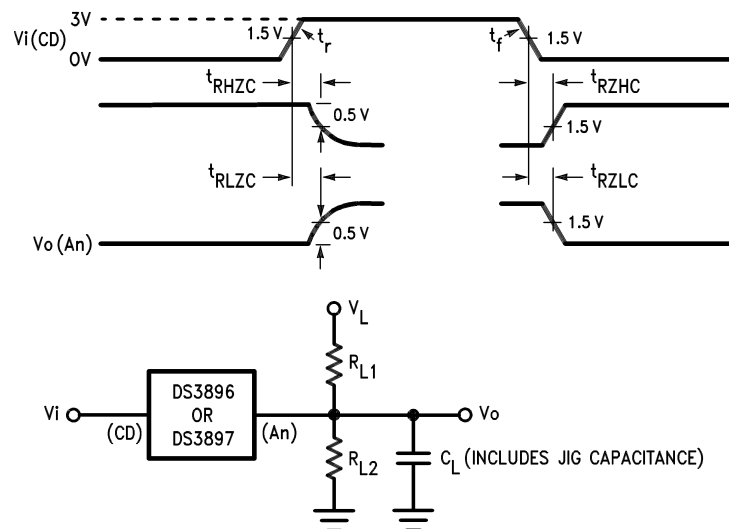
Note: t_r = t_f ≤ 5 ns from 10% to 90%

Figure 4. Driver Propagation Delays



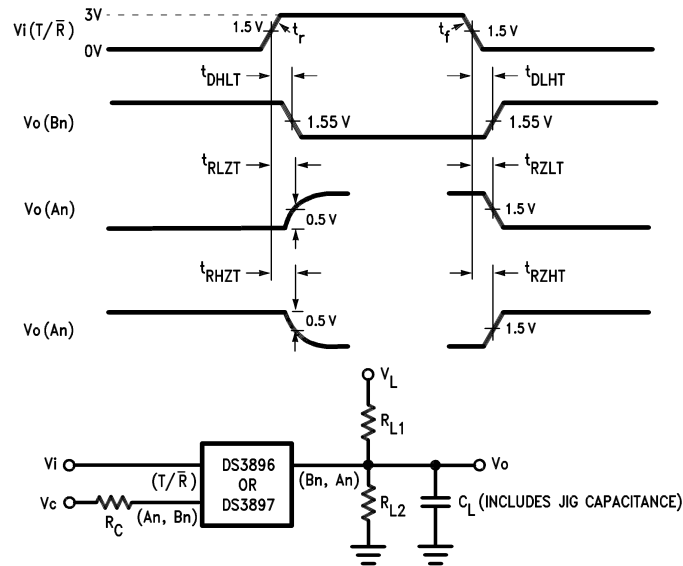
Note: $t_R = t_F \leq 10$ ns from 10% to 90%

Figure 5. Receiver Propagation Delays



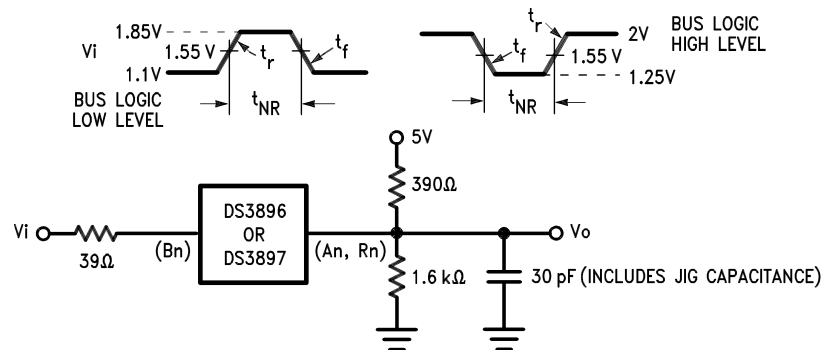
Note: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 6. Propagation Delay from CD pin to An



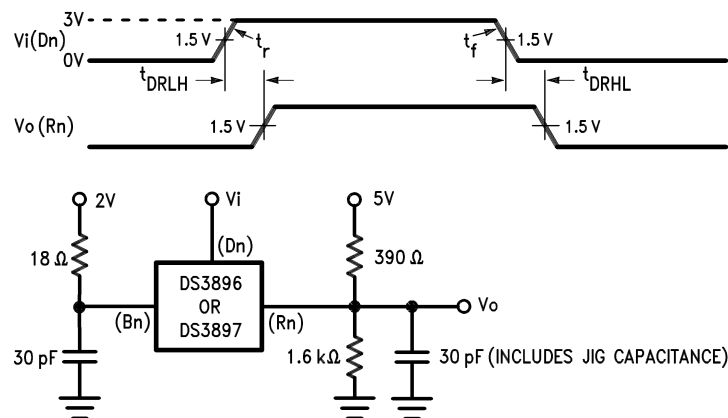
Note: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 7. Propagation Delay from T/R pin to An or Bn



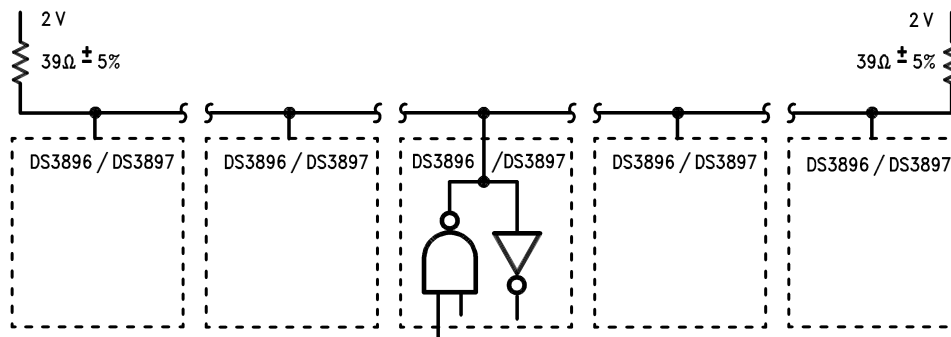
Note: $t_r = t_f = 2$ ns from 10% to 90%

Figure 8. Receiver Noise Immunity: "No Response at Output" Input Waveforms



Note: $t_r = t_f \leq 5$ ns from 10% to 90%

Figure 9. Driver Plus Receiver Delays

TYPICAL APPLICATION

REVISION HISTORY

Changes from Revision C (February 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	8

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